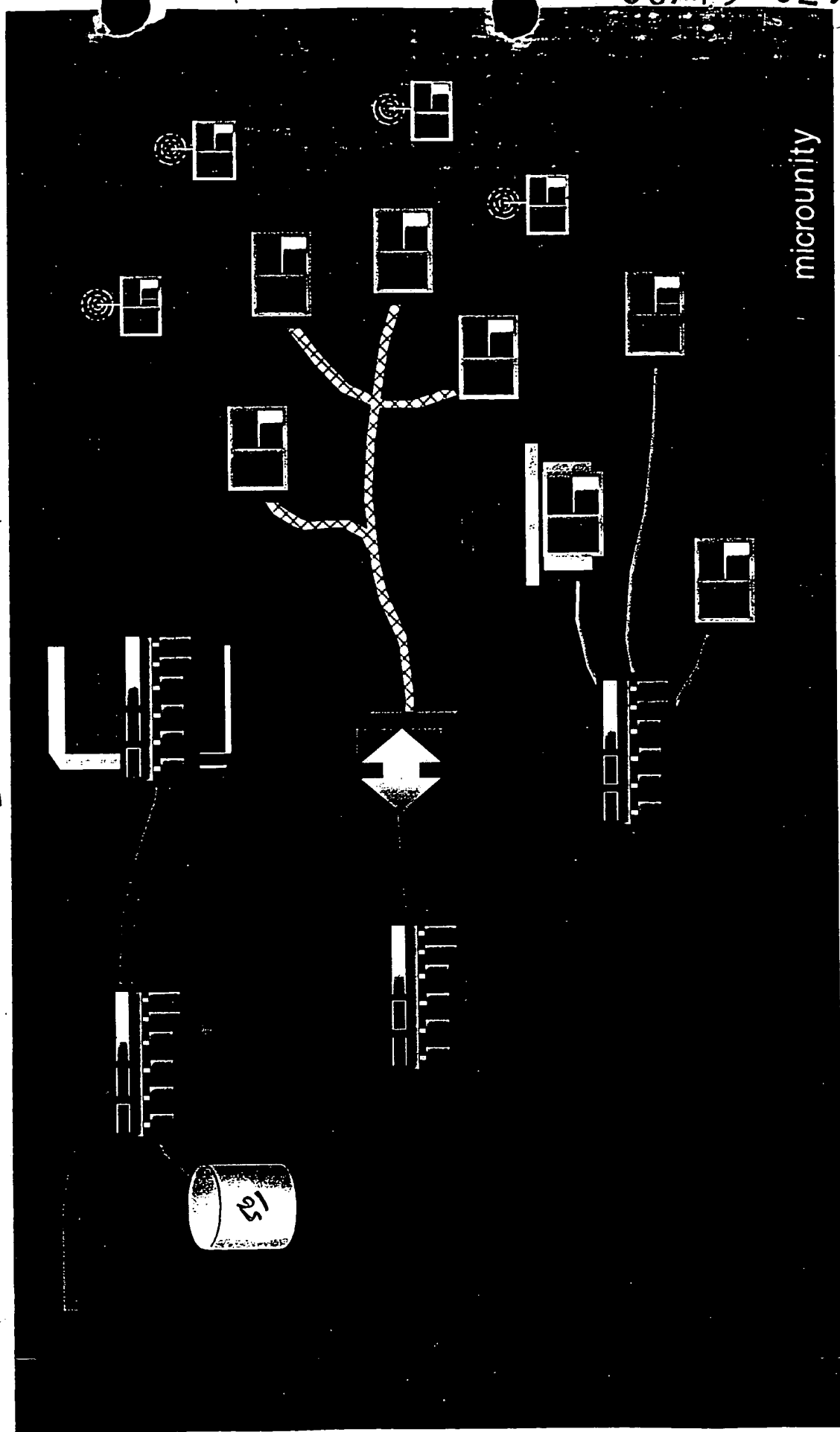


Figure 1

microunity

Figure 2



2001-0000-0000-0000

31

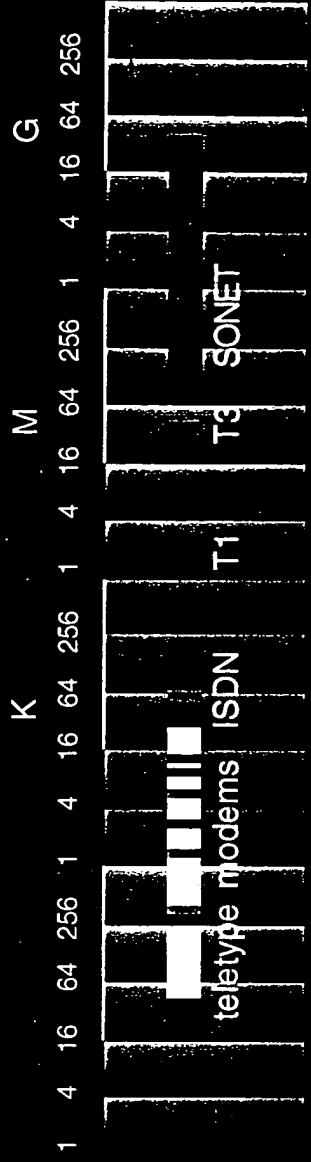
(BITS / SECOND)



Figure 4

(BITS / SECOND)

Telecom



Media

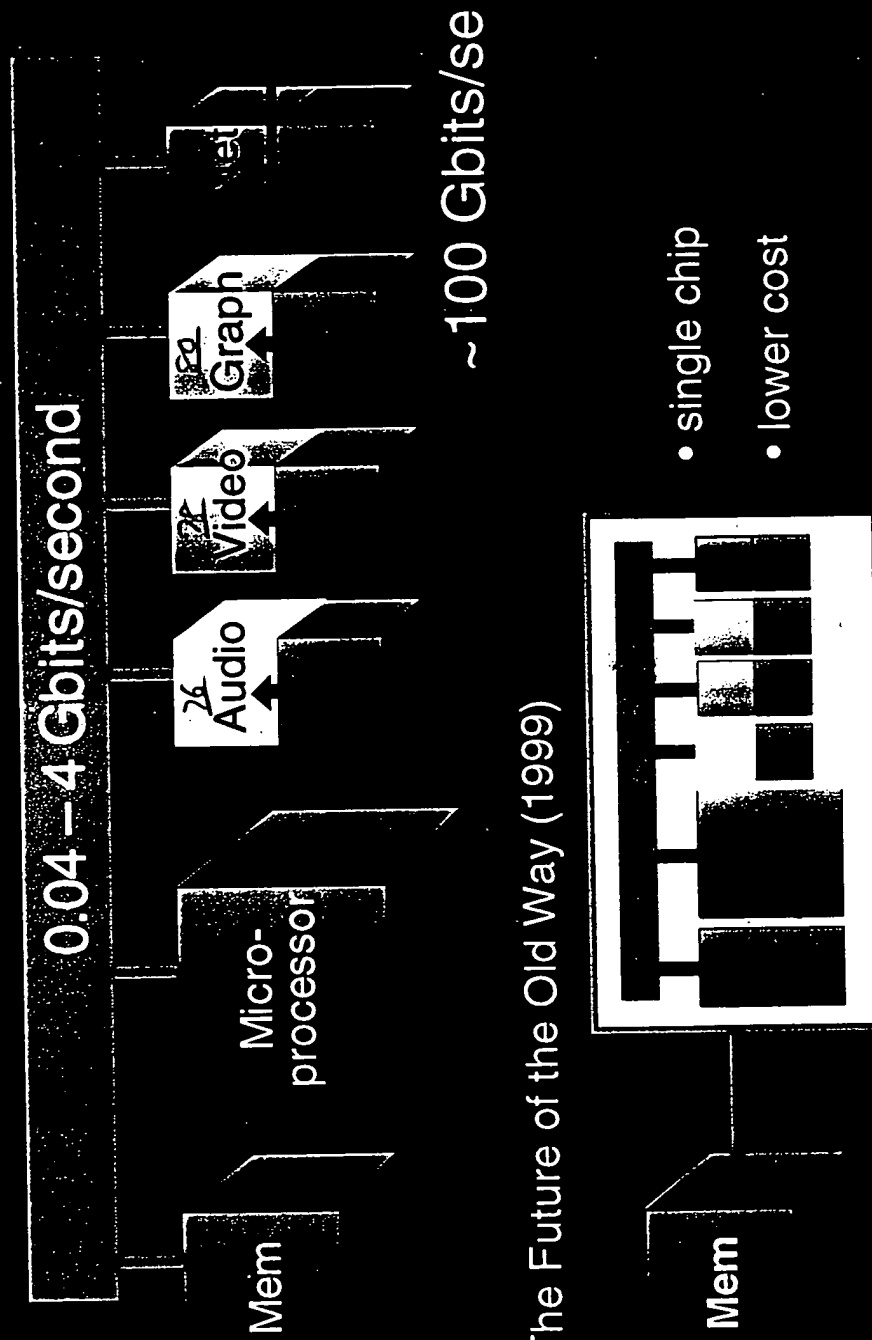


Computing



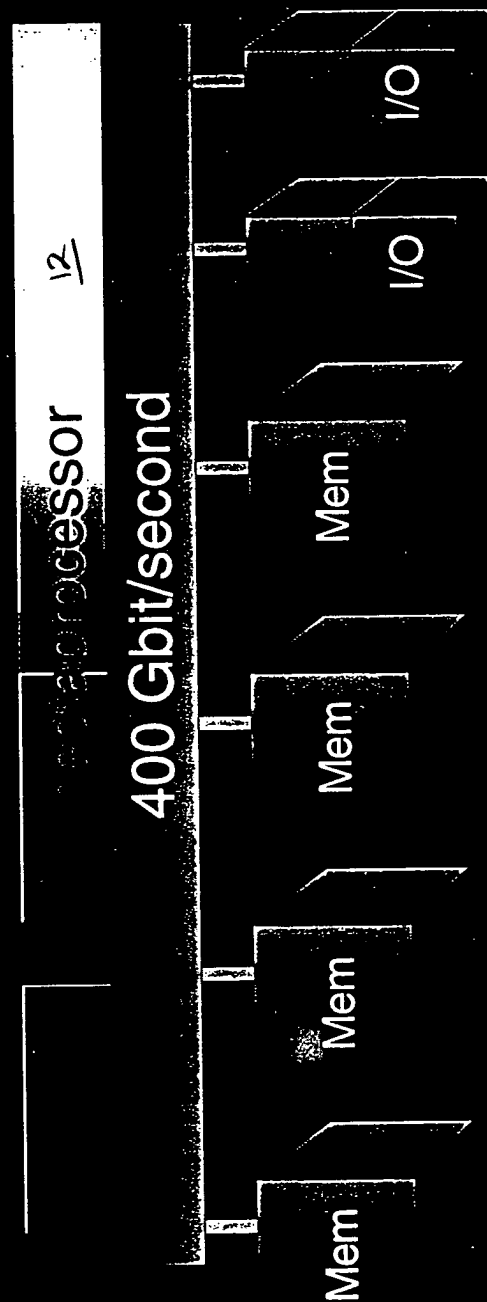
microunity

Figure 5

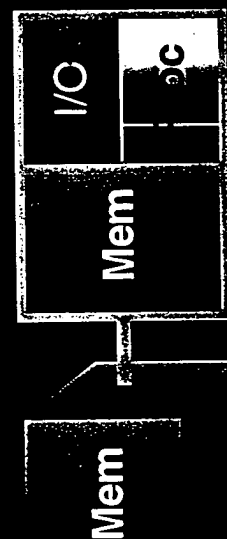


microcircuit

Figure 6



The Future of the Unified Way (1995)



- smaller chip
- much lower cost

2004-02-25-230

Figure 7

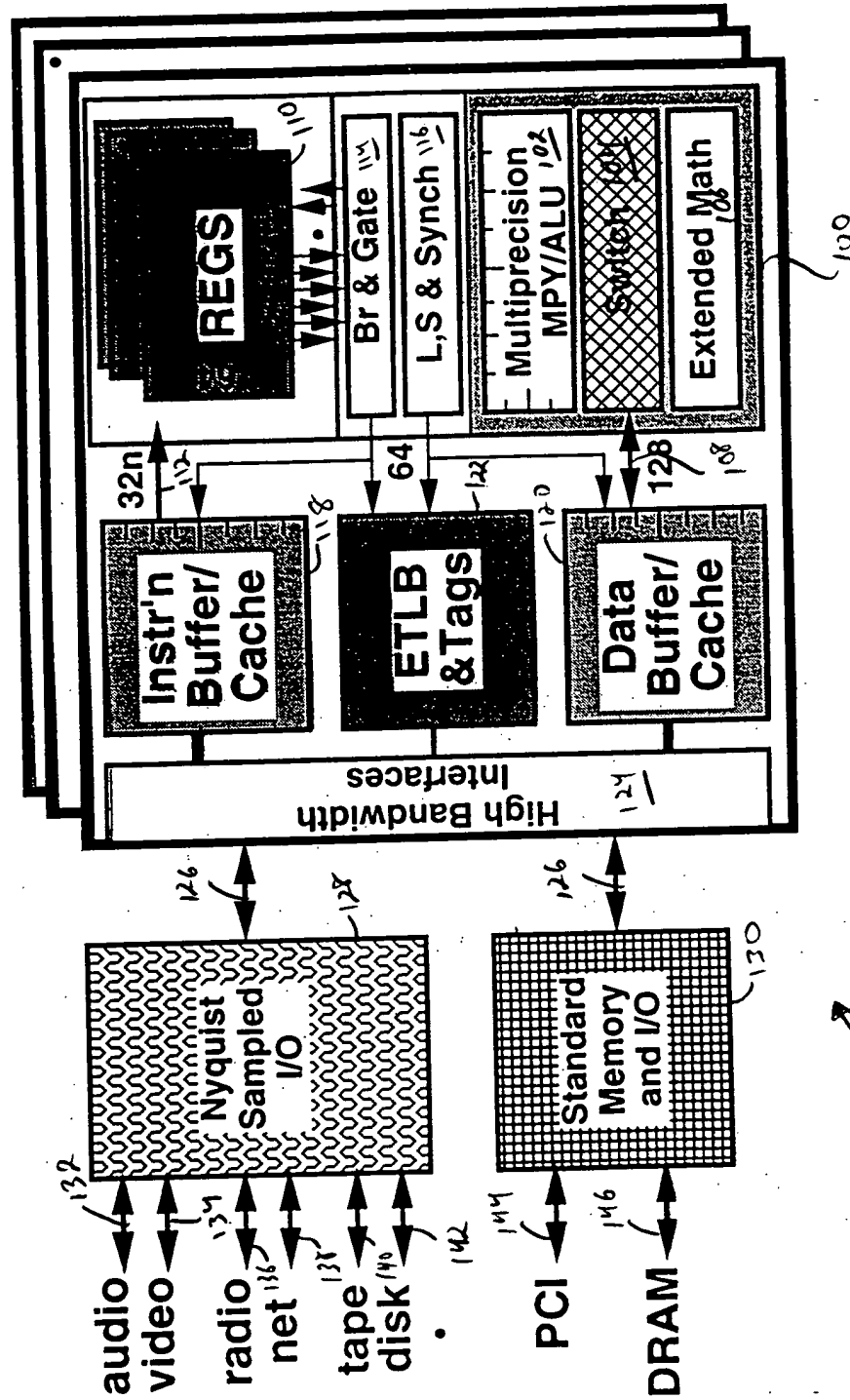


Figure 8(a)

Group Expand

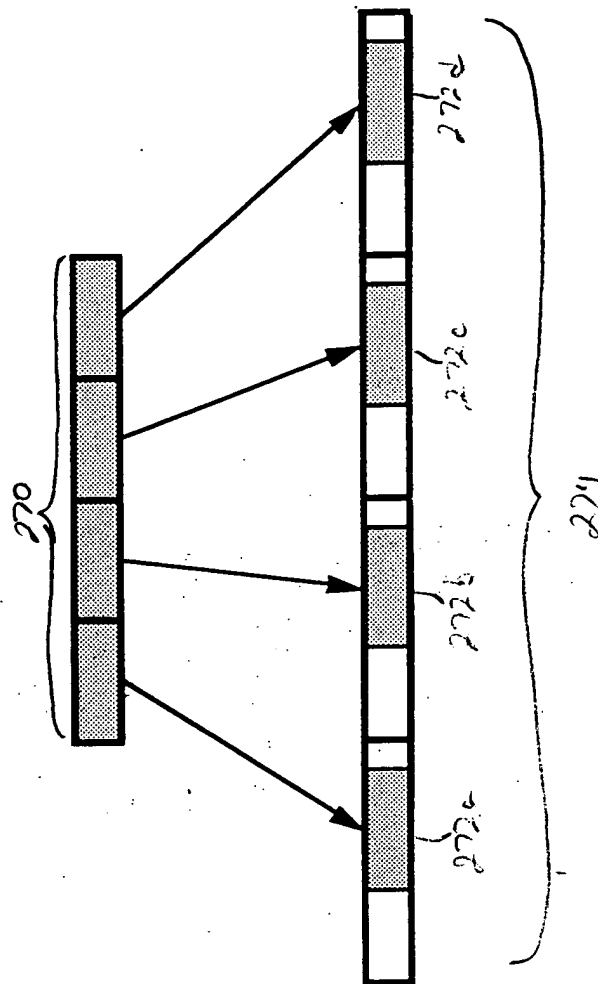


Figure 8(b)
Group Compress, Extract

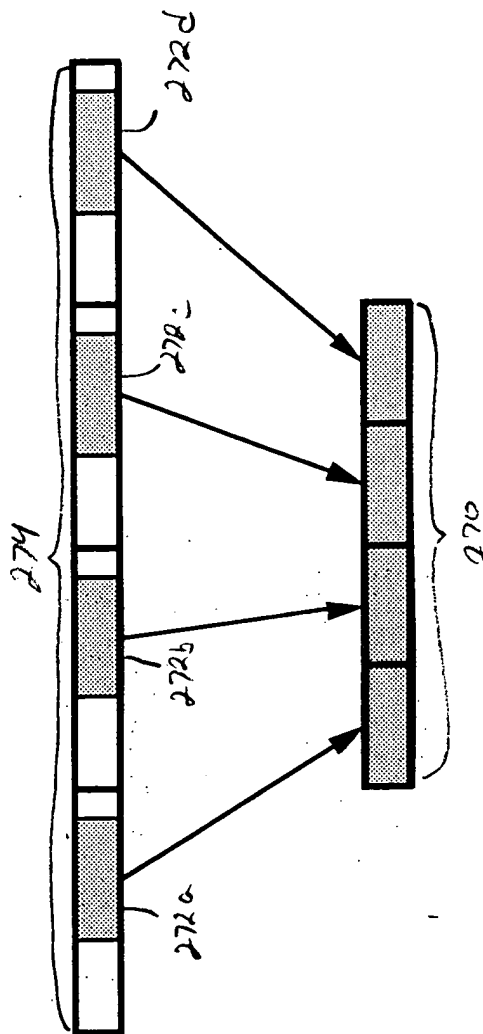
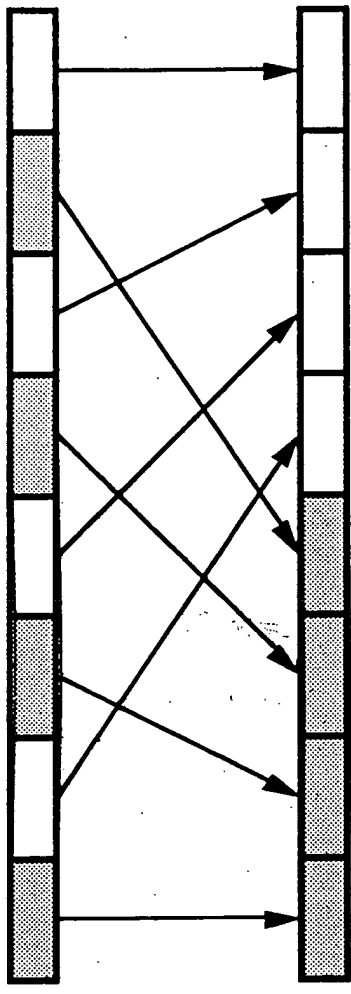


Figure 8(c)

Group Deal, Shuffle

- Group Deal: 128 bits to 128 bits



- Group Shuffle: 128 bits to 128 bits

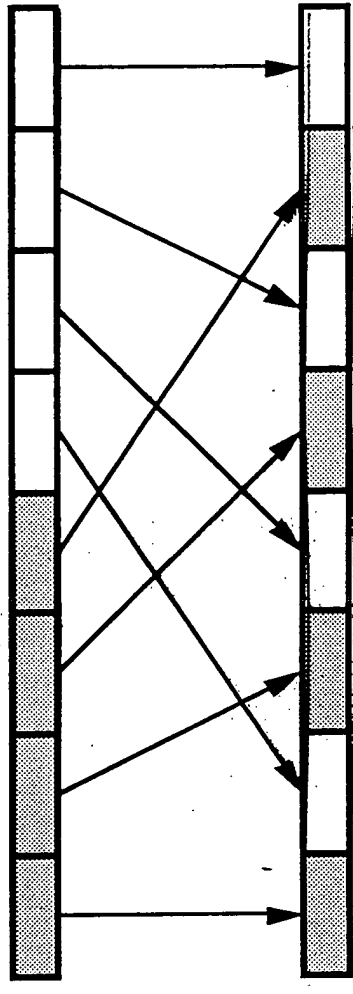


Figure 8(d)

Group Swizzle (Copy-Swap)

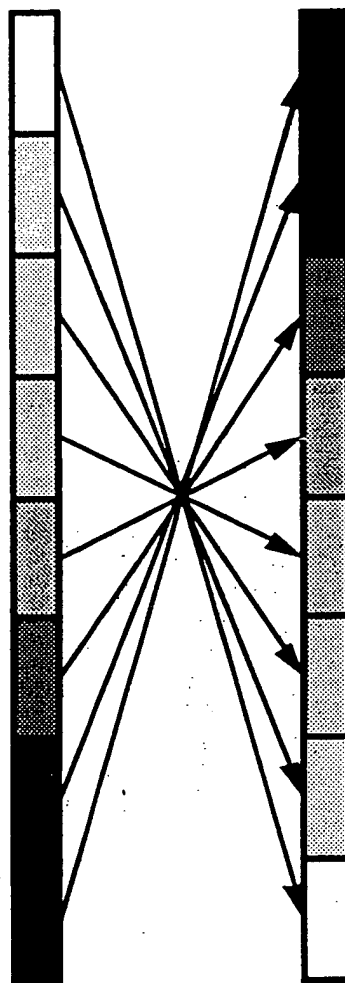


Figure 8(e)

Group Permute

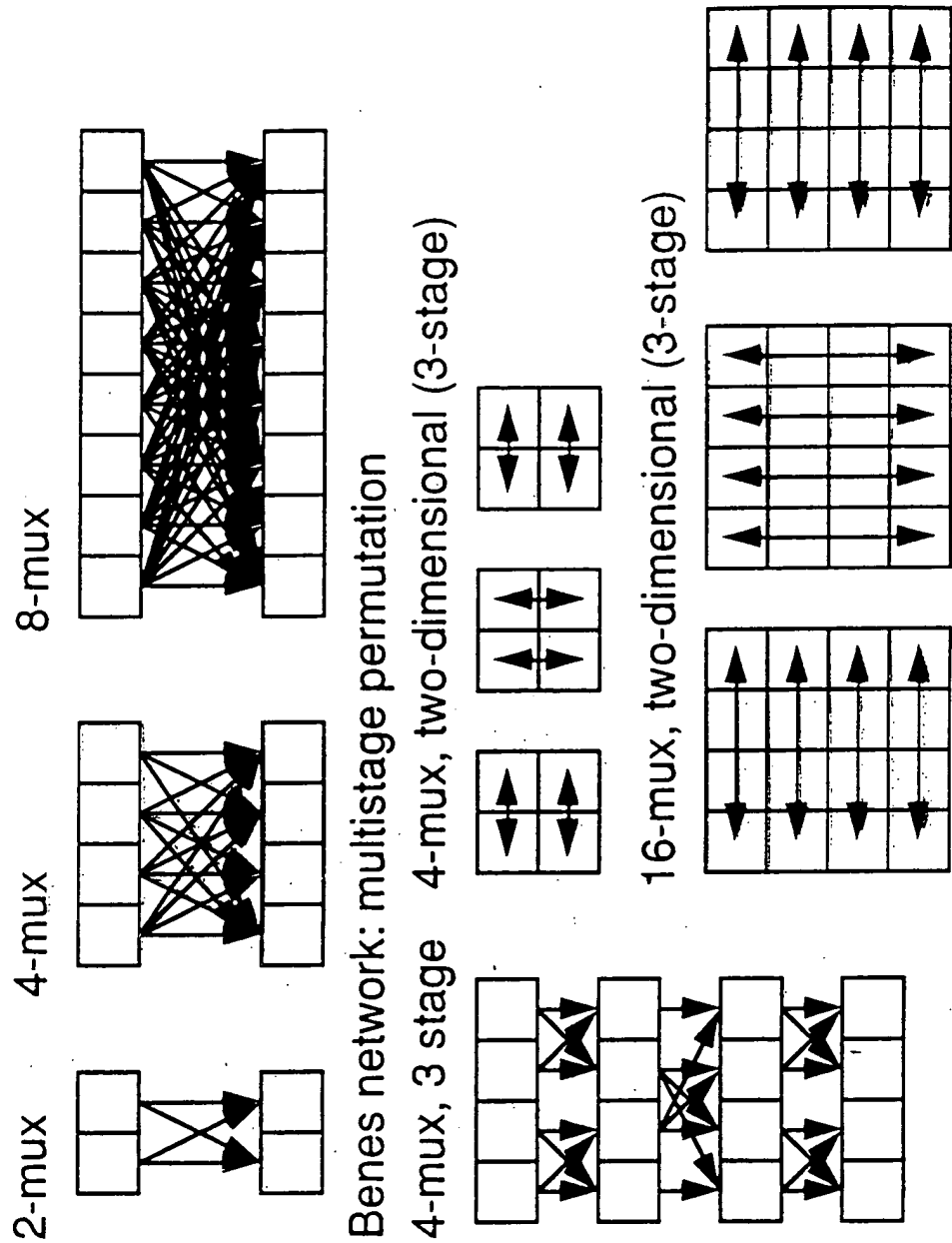


Figure 9(a)

Instruction Formats

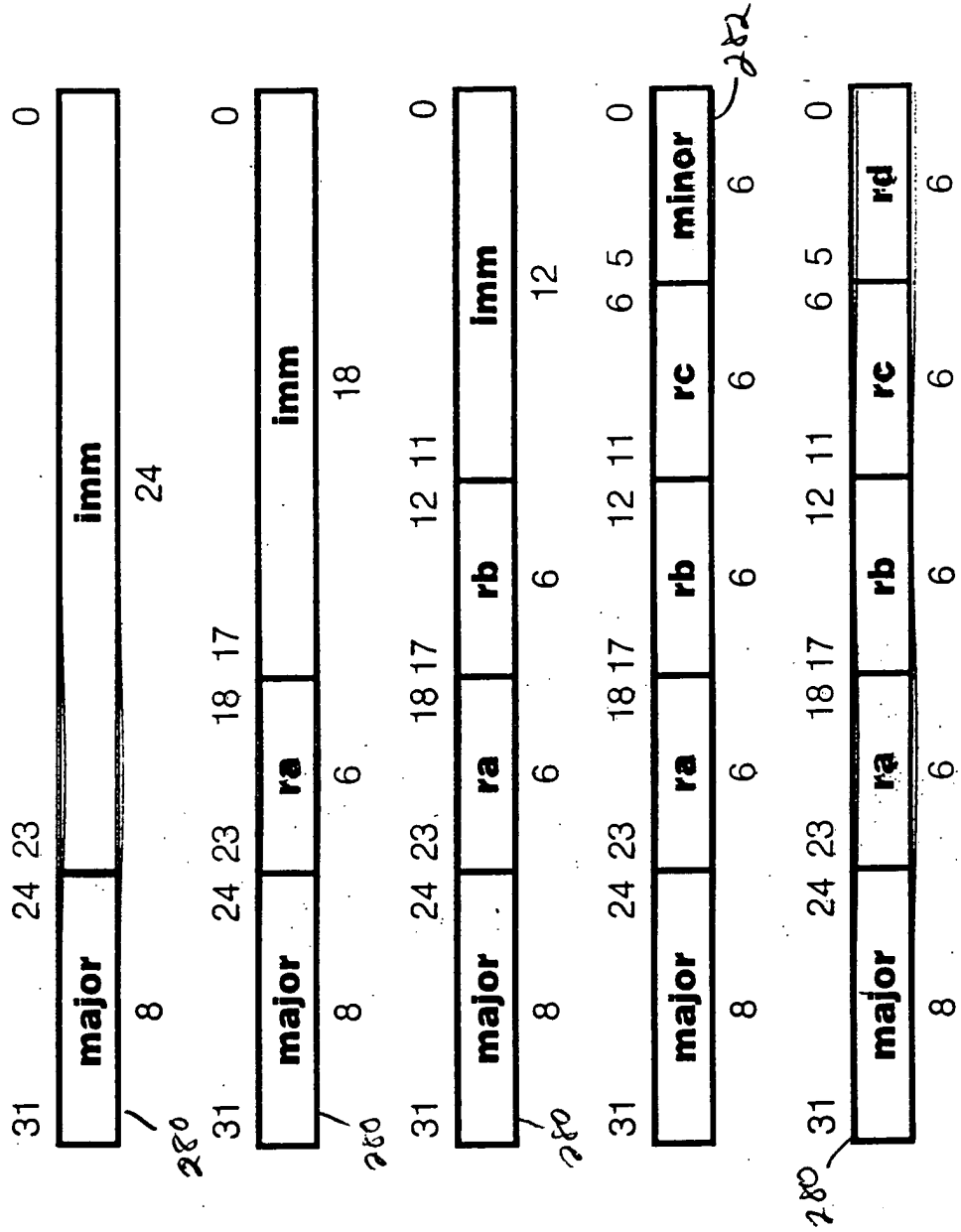


Figure 9(b)

Floating-point Data Sizes

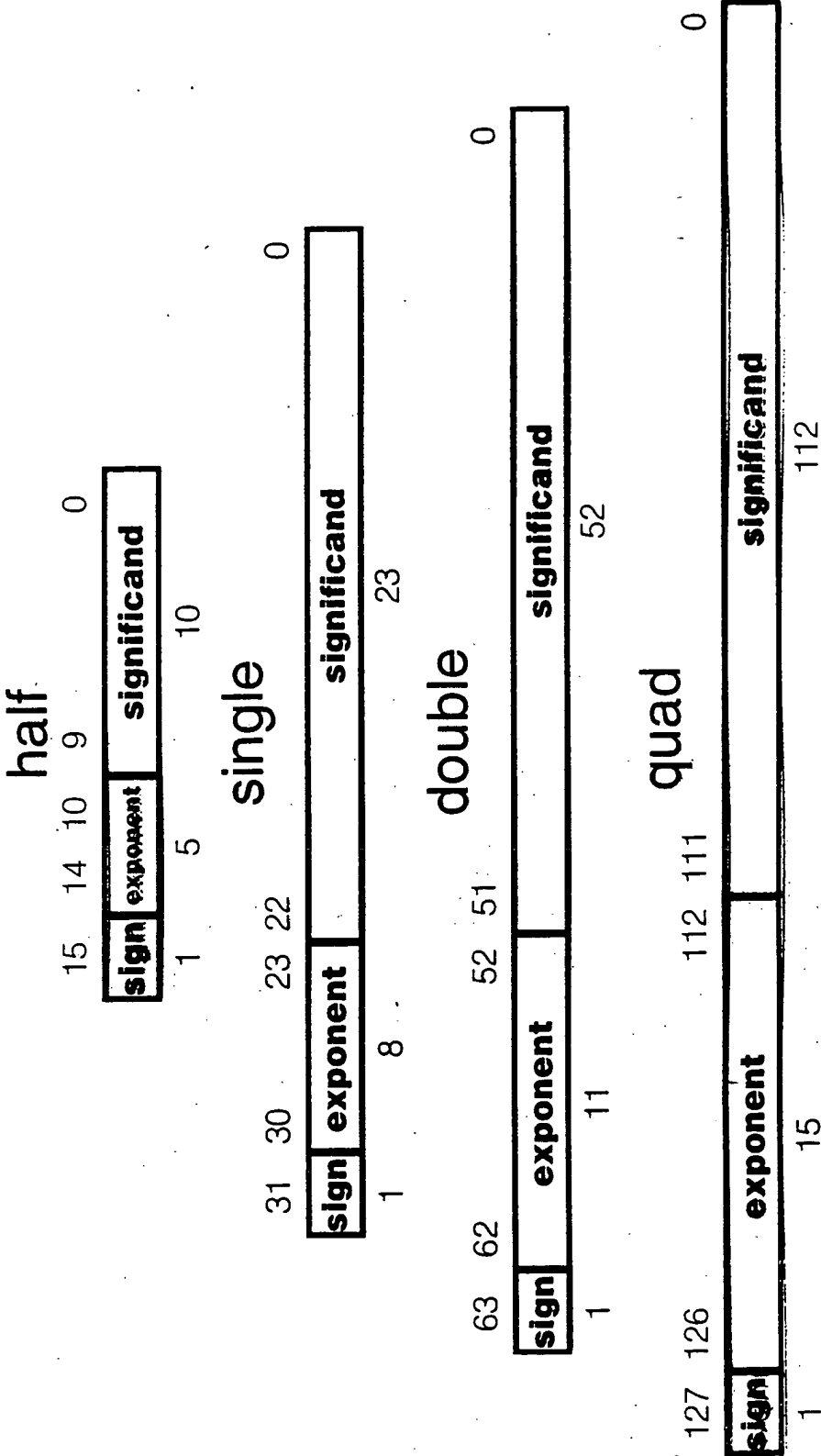


Figure 9(c)

Fixed-Point Data Sizes

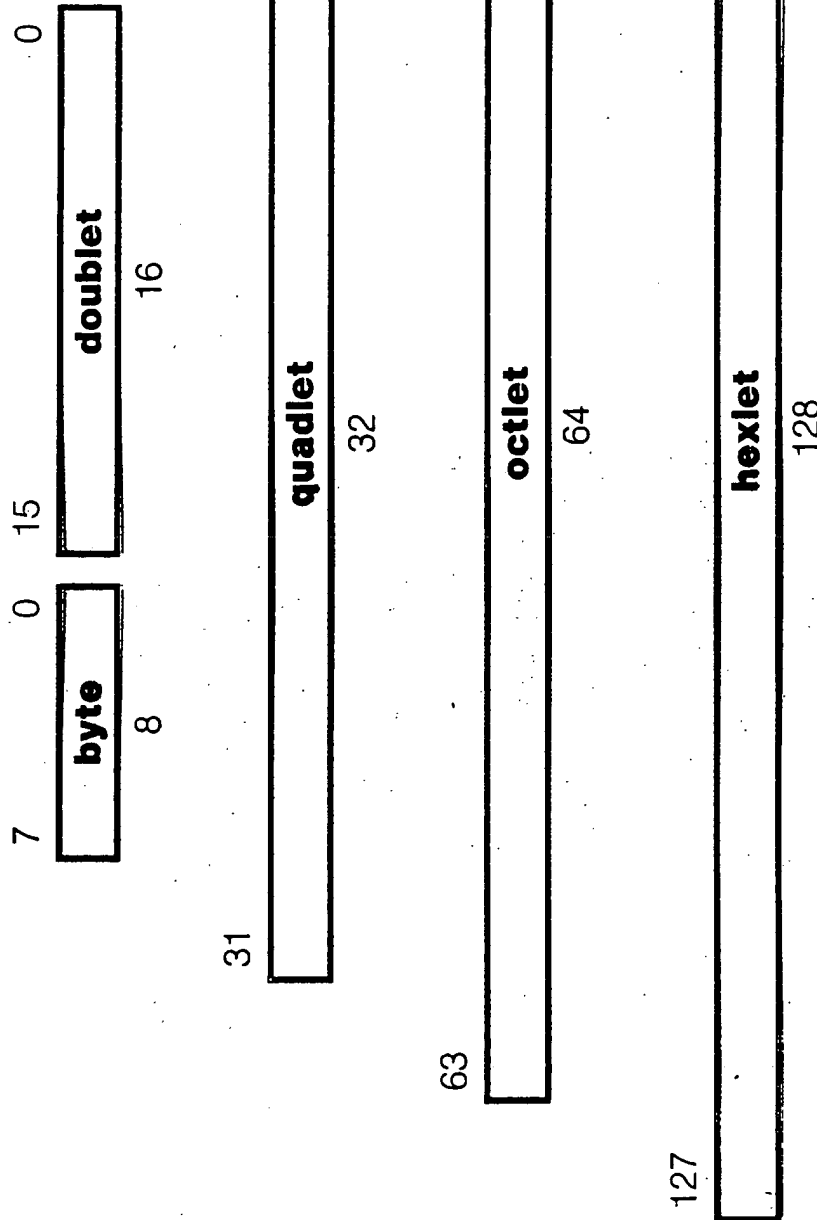


Figure 10(a)

Translation Block Diagram

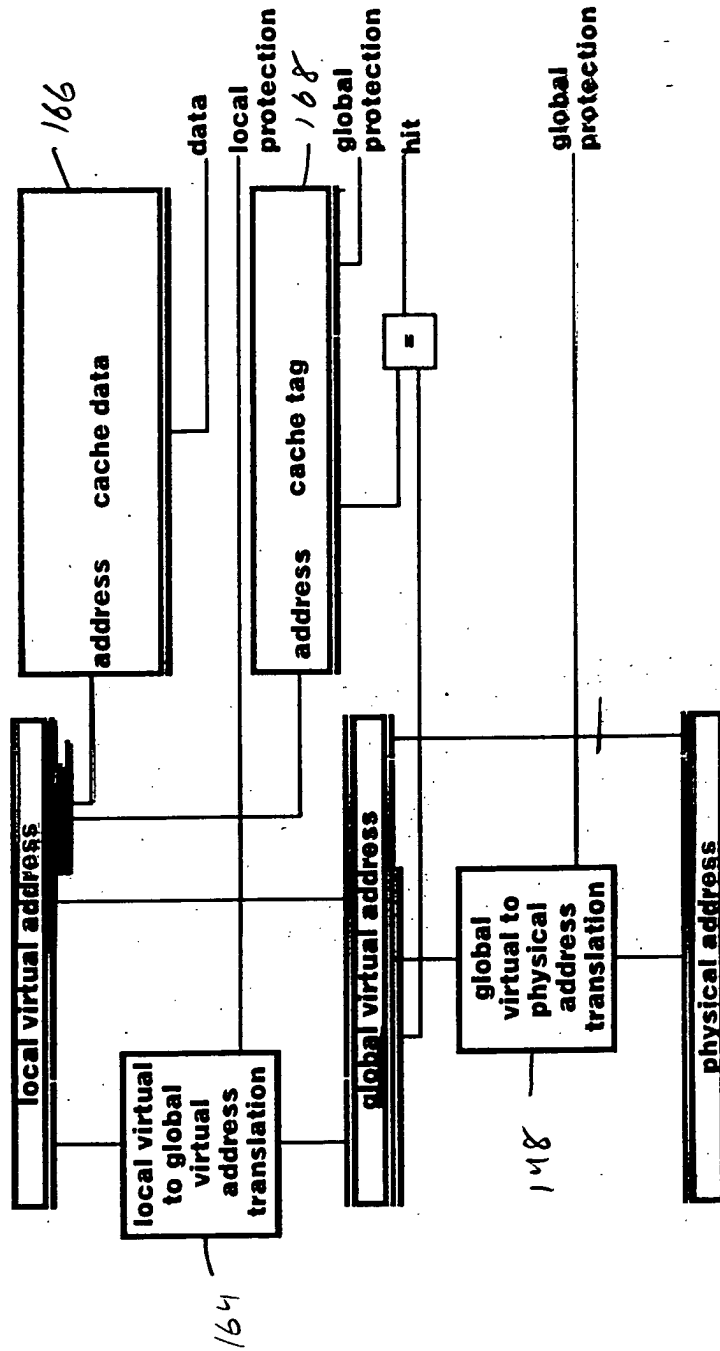


Figure 10(b)

Translation Lookaside Buffer

148

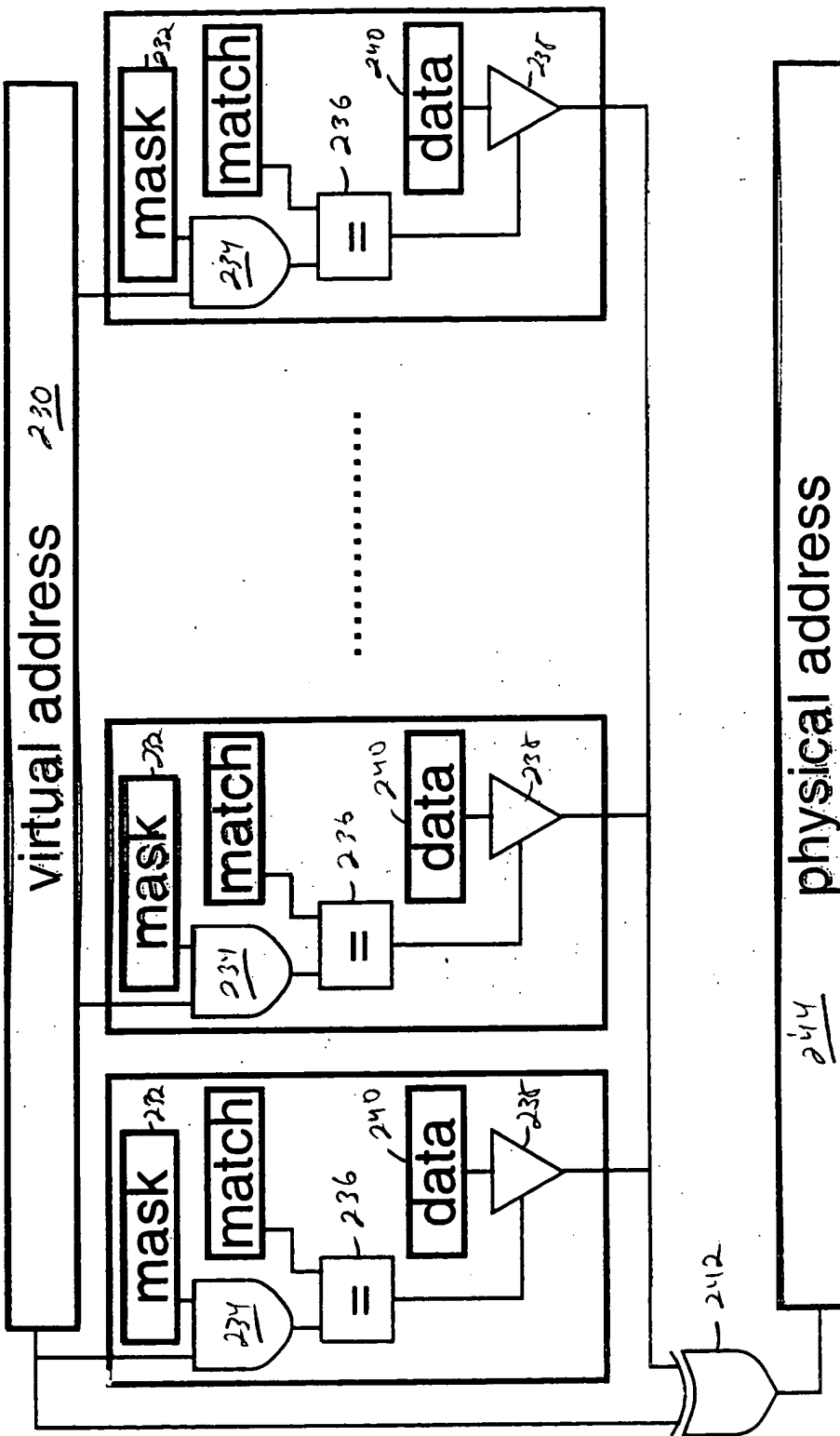


Figure 11

Superstring Pipeline

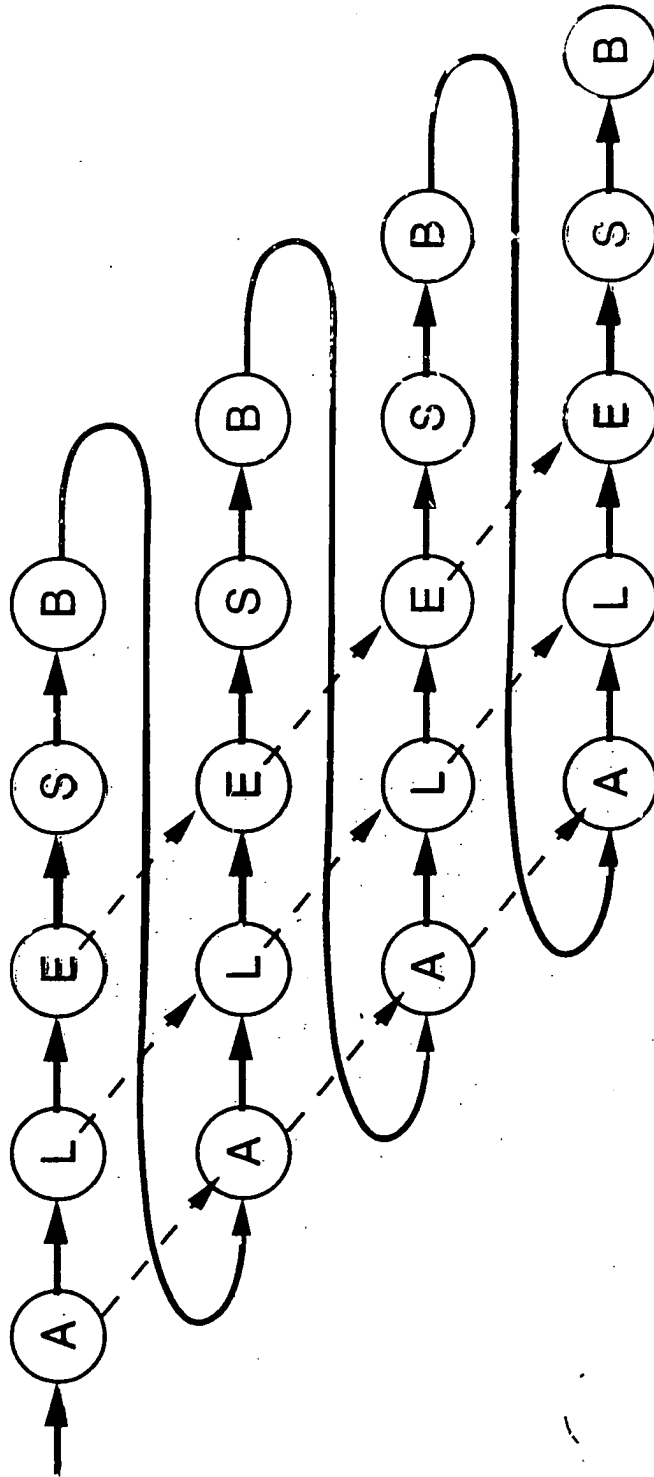


Figure 12

Superspring Pipeline

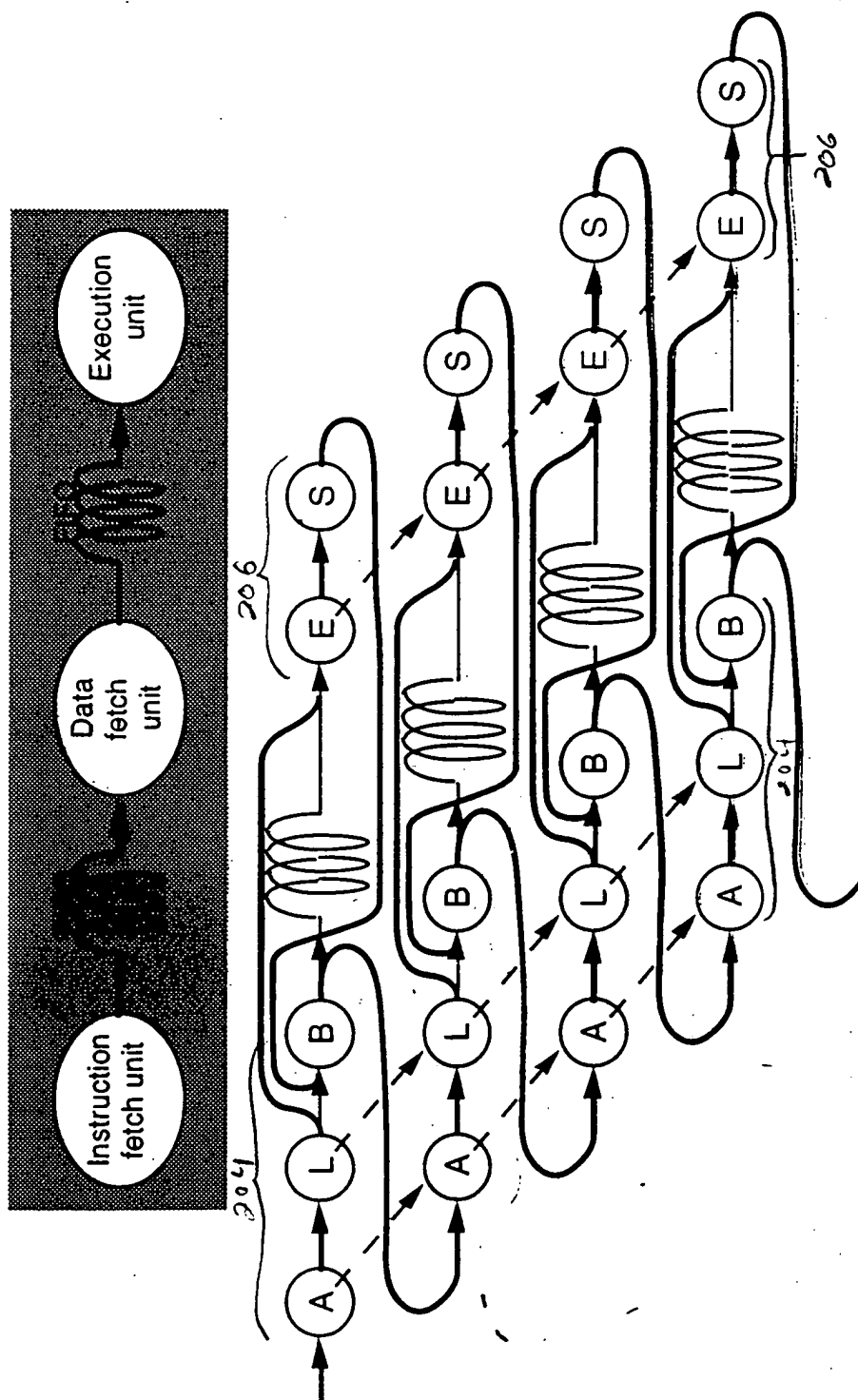


Figure 1 is a block diagram of a multi-processor system. It shows four identical processor units, each labeled 150. Each unit contains a 64 KByte Cache (156a) and a DRAM CTL (156b). The caches are connected to a common 72-bit data bus (160). Each processor also has its own 72-bit data bus (162) connected to its DRAMs (154). A 16-bit address bus (164) and a 4-bit control bus (166) are also shown.

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Figure 14

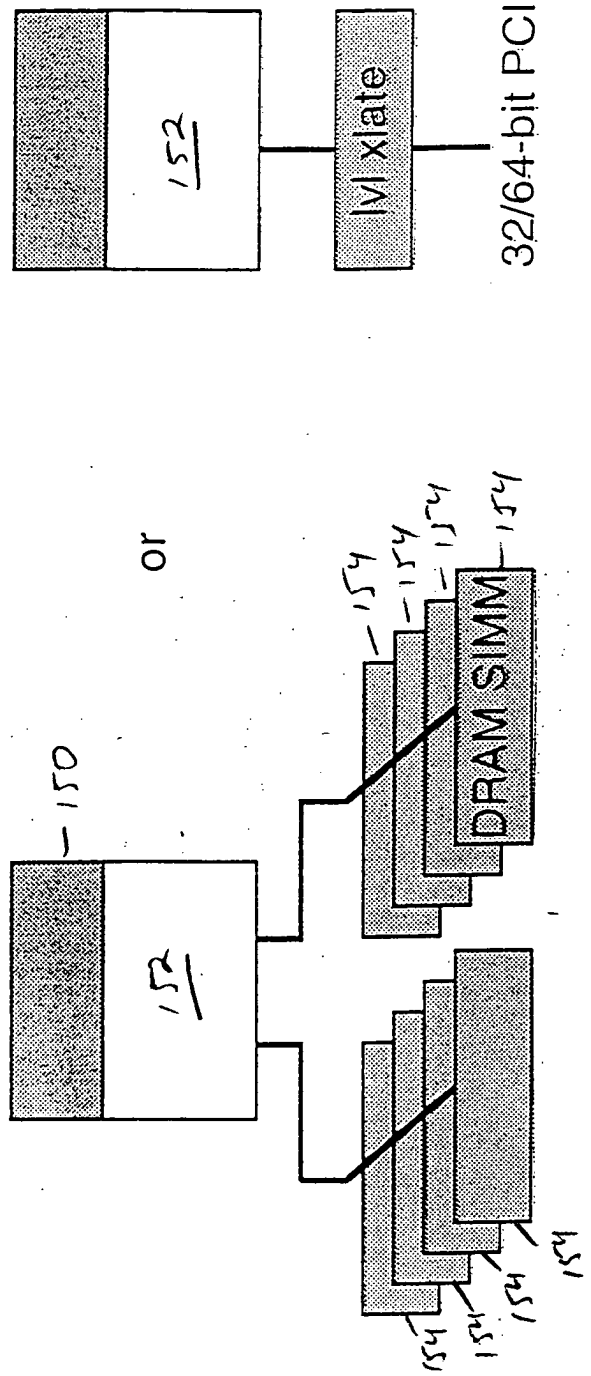


Figure 15

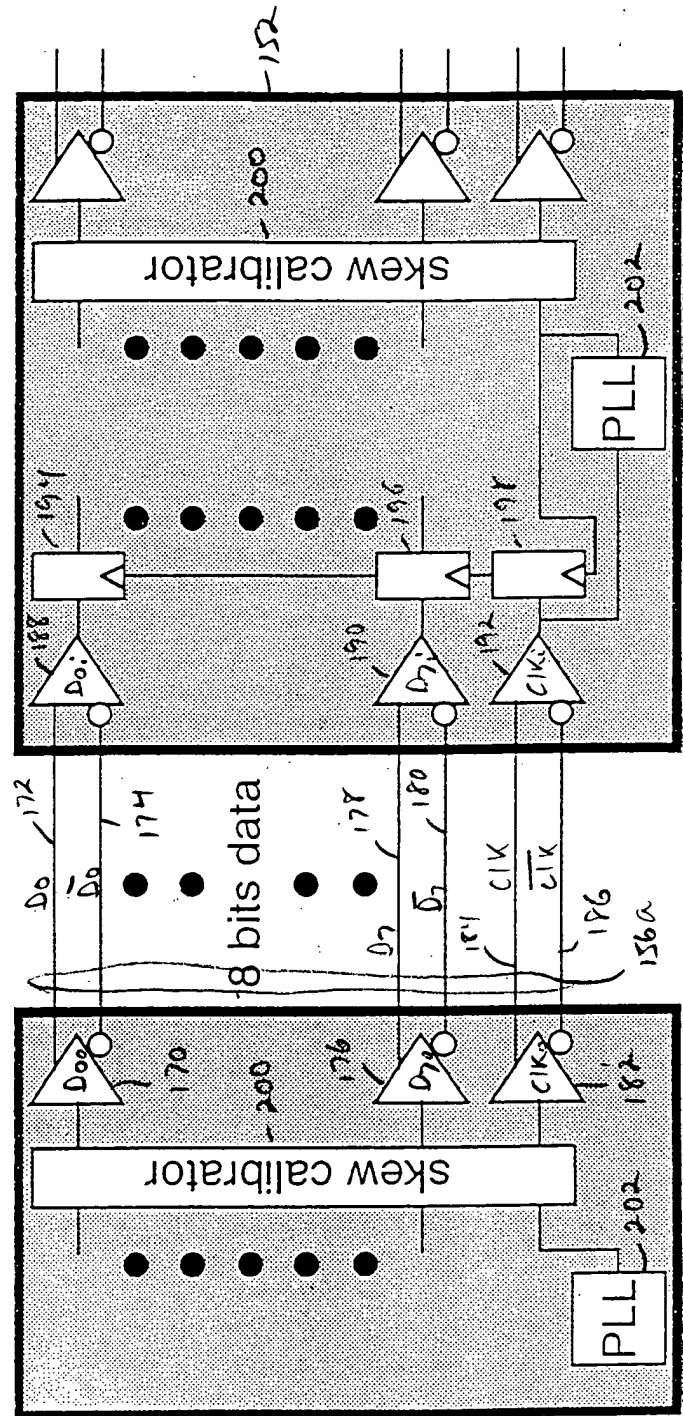
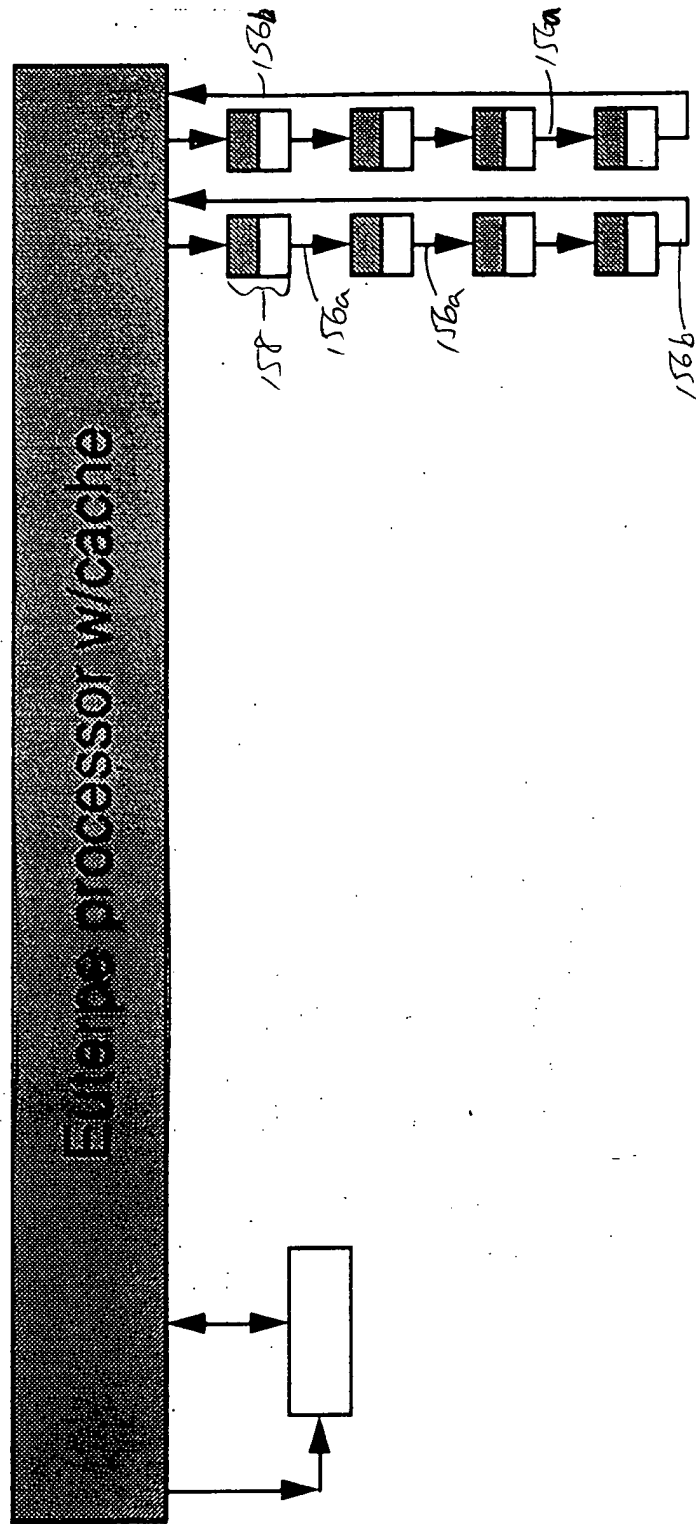
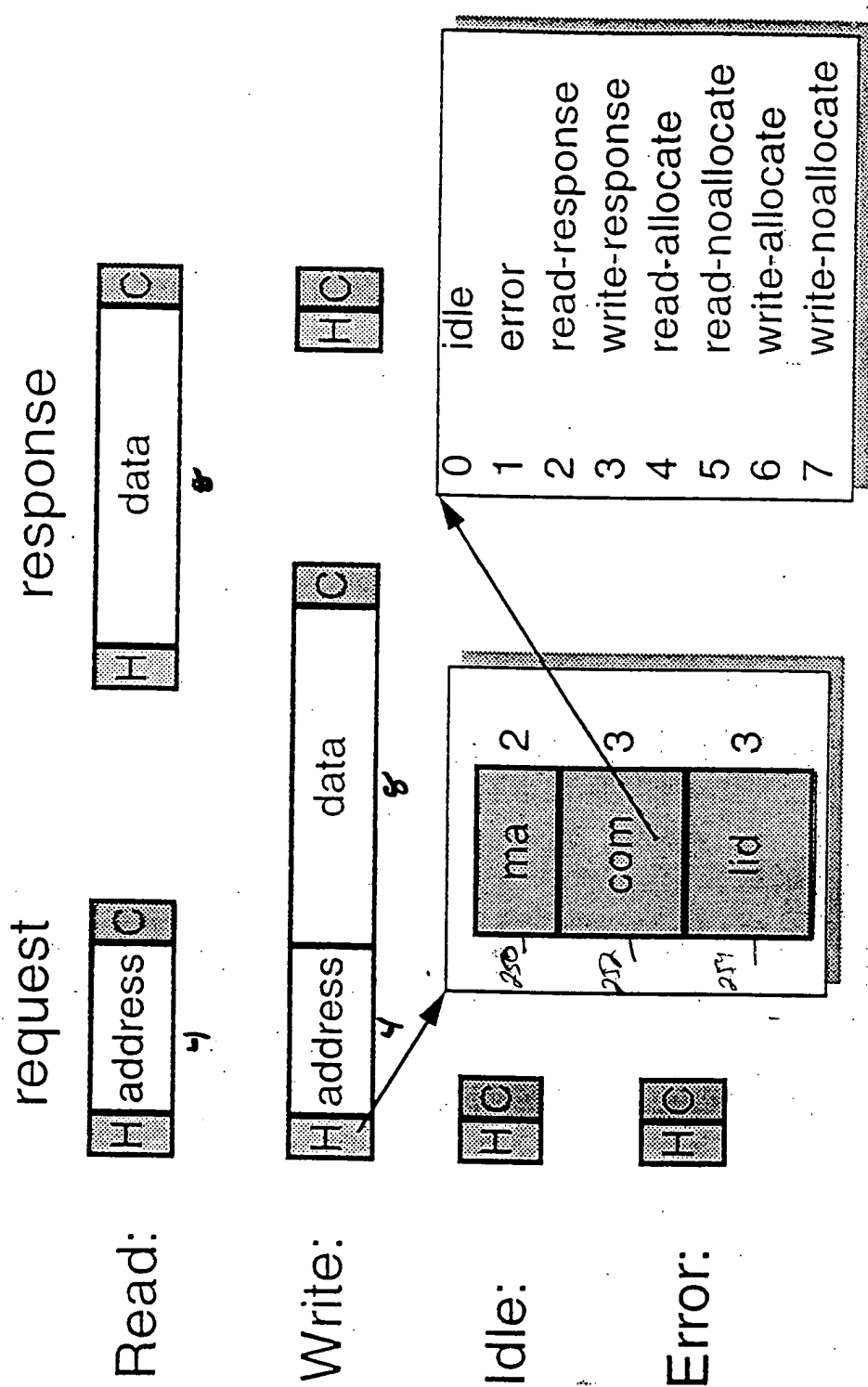


Figure 16(a)



[illegible]

Figure 17



450120 DASH 400

Figure 18

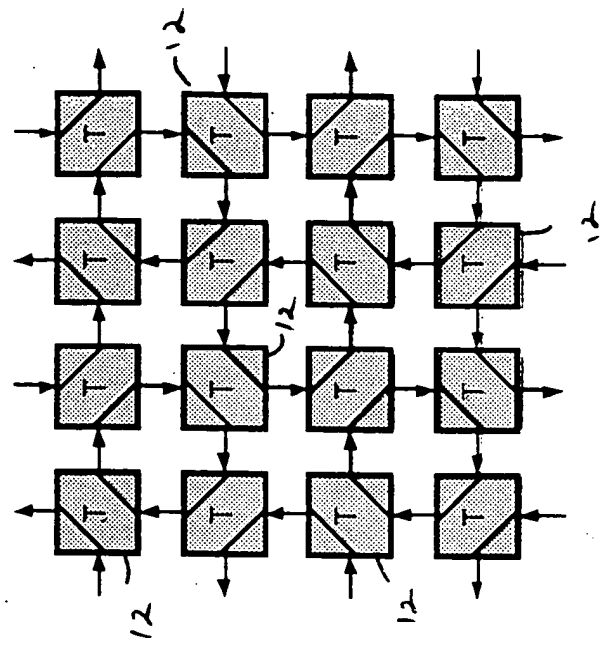
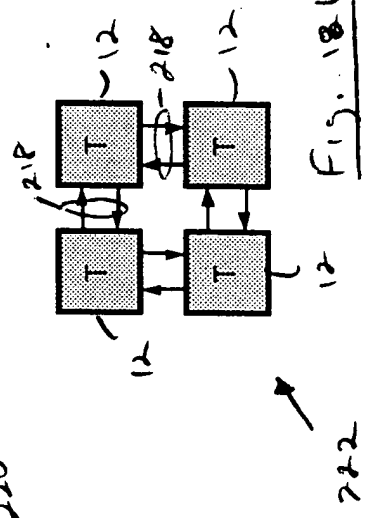
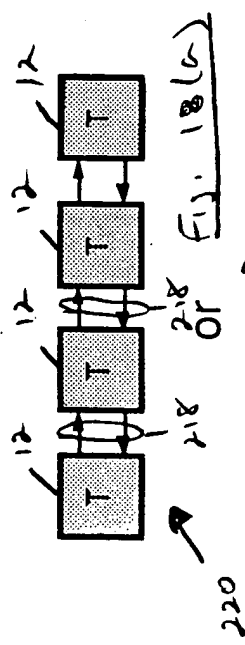
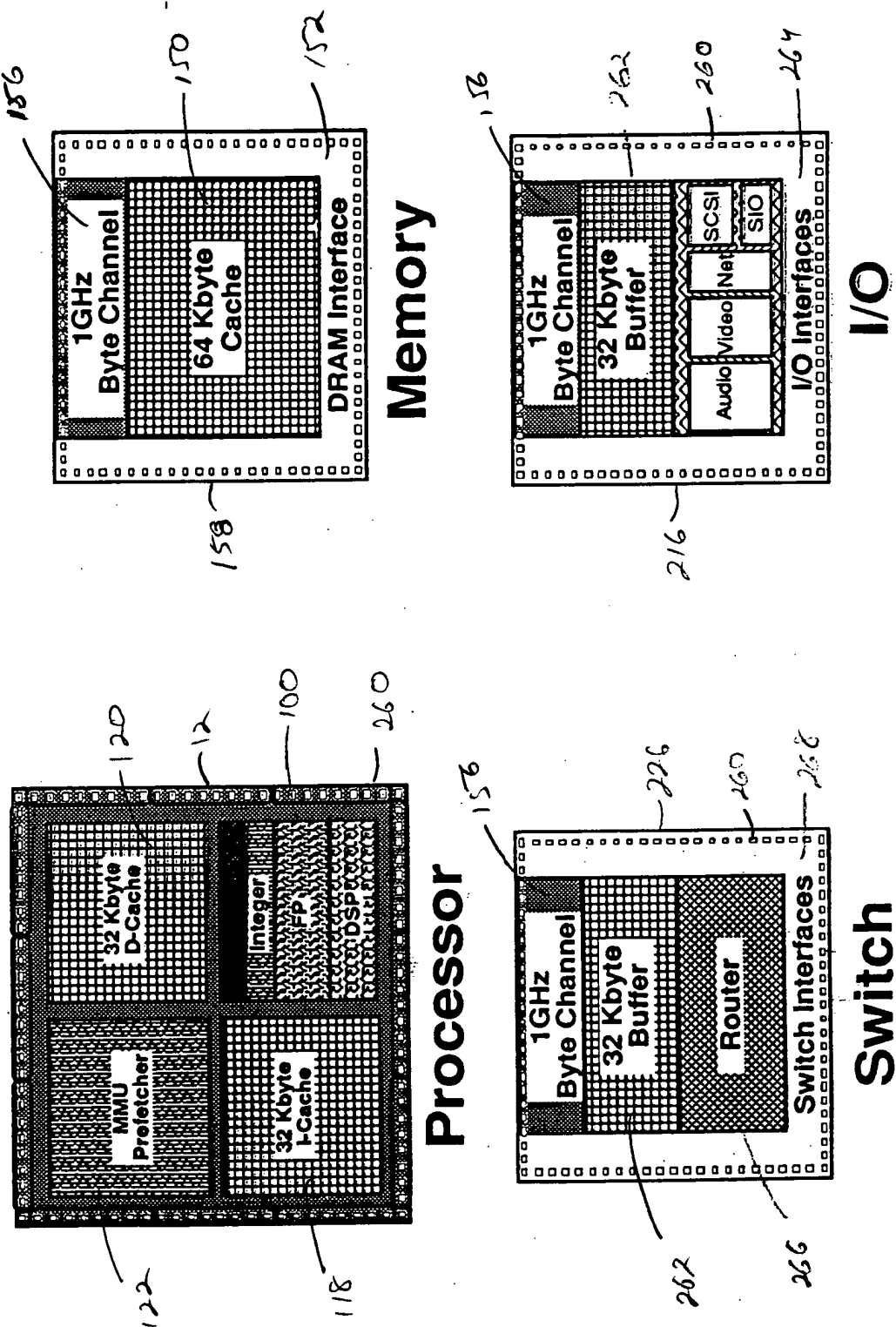


Figure 19



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